ELEC9451 / ELEC4951

THE UNIVERSITY OF NEW SOUTH WALES

School of Electrical Engineering
and Telecommunications

THESIS/PROJECT PART A
TECHNICAL REPORT COVER-SHEET

Study the marking guide and the requirements given overleaf. Complete the details required on this form and include it at the front of your report (first page).

Student name: Jamie Mo **Student ID:** z53634317

Thesis/Project title: Adaptive Impedance Matching Transmit Driver in 22nm CMOS

Supervisor: Torsten Lehmann **Assessor:** _____

I declare that this assessment item is my own work, except where acknowledged, and has never been submitted for academic credit elsewhere, and acknowledge that the assessor of this item may, for the purpose of assessing this item,

(i) reproduce this assessment item and provide a copy to another member of the University, and/or

(ii) communicate a copy of this assessment item to a plagiarism checking service (which may then retain a copy of the assessment item on its database for the purpose of future plagiarism checking).

I certify that I have read and understood the University Rules about Student Academic Misconduct.

Signature: _____ **Date**: 18/11/2024

SCHOOL OF ELECTRICAL ENGINEERING
AND TELECOMMUNICATIONS

Adaptive Impedance Matching Transmit Driver in 22nm CMOS

by

Jamie Mo

Student ID: z5364317

Thesis submitted as a requirement for the degree

Bachelor of Engineering (Electrical Engineering)

Submitted: November 18, 2024
Supervisor: Torsten Lehmann

Abstract

This document explores the design of a circuit for dynamically adjusting the output impedance of a transmit driver in a 22nm CMOS process. Initial research has focused on understanding impedance matching challenges, exploring existing solutions, developing a preliminary design for the sensing mechanism, and conducting simulations to verify feasibility. Early results indicate the potential to detect impedance mismatch, laying the groundwork for further development.

Acknowledgements

I wish to thank all the people who have guided me in this project; in particular Torsten Lehmann and Tim Robins.

Abbreviations

CMOS Complementary Metal-Oxide-Semiconductor

PVT Process, Voltage, and Temperature

VSWR Voltage Standing Wave Ratio

S-Parameters Scattering Parameters

ISI Intersymbol Interference

FIR Finite Impulse Response

ADC Analog-to-Digital Converter

DSP Digital Signal Processing

VNA Vector Network Analyzer

TDR Time-Domain Reflectometry

EMI Electromagnetic Interference

VML Voltage-Mode Logic

CML Current-Mode Logic

PLL Phase-Locked Loop

SPICE Simulation Program with Integrated Circuit Emphasis

Contents

Chapter 1

Introduction

1.1 Context

A primary factor affecting signal integrity in high-speed digital systems is impedance mismatch between the output driver and the connected transmission line or load. Ensuring matched impedance is crucial for reliable data transmission, as unmatched impedance causes signal reflections that degrade transmission quality [1]. This issue becomes even more critical at gigahertz frequencies, where tighter timing margins make systems highly sensitive to even minor distortions, which can significantly compromise data accuracy [2].

Furthermore, integrated circuits manufactured in advanced CMOS nodes, such as 22nm, become increasingly susceptible to variations due to process, voltage and temperature (PVT) [3]. These variations can cause substantial deviations in device parameters, making it challenging to maintain a stable output impedance. As a result, an adaptive impedance matching mechanism can be an effective approach to addressing these challenges.

1.2 Problem Statement

An existing transmit driver design requires a mechanism to dynamically adjust its output impedance to match its connected line and load, minimizing signal reflections and ensuring high data integrity. Achieving this impedance matching is challenging due to the on-chip implementation, limited control options, and high-frequency operation, while still requiring a solution that is both precise and responsive.

Chapter 2

Theoretical Background

This chapter provides the theoretical background necessary for understanding the problem.

2.1 Impedance Matching

Impedance matching is designing source and load impedances to minimize signal reflection or maximize power transfer. Reflections cause destructive interference, leading to peaks and valleys in the voltage. There are two types of impedance matching: conjugate matching and reflectionless matching, the difference concerning the imaginary component of the impedance [4].

Conjugate Matching

In conjugate matching, the source impedance Z_S is made the complex conjugate of the load impedance Z_L, which maximizes power transfer by canceling out reactive components:

$$Z_S = Z_L^* = R_L - jX_L \tag{2.1}$$

Reflectionless Matching

In reflectionless matching, Z_S is matched directly to the characteristic impedance of the load or transmission line Z_L, which is typically a real value to minimize signal reflections:

$$Z_S = Z_L \tag{2.2}$$

2.2 Transmission Lines

It's important to achieve an intuitive and physical understanding of how a transmission line behaves to achieve proper impedance matching and termination. Transmission lines are modeled using distributed parameters, which represent values per unit length. These parameters influence how signals propagate through the line [5].

Characteristic Impedance

The characteristic impedance, Z_0, of a transmission line determines the transmission efficiency of the signal. It is defined by the line's inductance L and capacitance C per unit length:

$$Z_0 = \sqrt{\frac{L}{C}}$$

Reflection Coefficient

For efficient transmission, the driver and load impedances must match Z_0. When there is a mismatch, part of the signal reflects back toward the source, causing interference. Reflection is quantified by the reflection coefficient Γ:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

where Z_L is the load impedance.

Scattering Parameters

Scattering parameters, or S-parameters, are commonly used to characterize the performance of high-frequency transmission lines. In particular, S_{11} and S_{21} are relevant for analyzing reflections and transmission [6]:

- S_{11} **(Reflection Coefficient** Γ**)**: The ratio of reflected to incident voltage, indicating the proportion of the input signal reflected back:

$$S_{11} = \Gamma = \frac{V_{\text{reflected}}}{V_{\text{incident}}}$$

- S_{21} **(Forward Transmission/Insertion Gain)**: The ratio of transmitted to incident voltage, describing the efficiency of the transmission.

$$S_{21} = \frac{V_{\text{transmitted}}}{V_{\text{incident}}}$$

Return Loss and Insertion Loss

Return Loss quantifies the signal power reflected back to the source. Higher return loss values indicate better impedance matching and fewer reflections. It is expressed in decibels (dB) as:

$$\text{Return Loss} = -20\log|S_{11}|$$

Insertion Loss describes the power lost as the signal travels along the transmission line, defined as the decrease in signal power between the input and output. Higher insertion loss values indicate greater power loss along the transmission line. It is expressed as:

$$\text{Insertion Loss} = -20\log|S_{21}|$$

2.3 Transmit Equalization

The performance of digital systems is largely limited by the interconnection bandwidth between devices. Even good current-mode signalling methods with matched terminations and carefully controlled line and connector impedance are limited to about 1GHz by the frequency-dependent attenuation of copper lines. Transmit equalization can help mitigate signal degradation caused by these losses [7].

High-Frequency Losses

As signals travel through transmission lines, higher-frequency components are more susceptible to attenuation and distortion than lower frequencies. This frequency-dependent degradation is caused by factors such as the skin effect and dielectric losses in the transmission medium [8].

Intersymbol Interference

Intersymbol interference (ISI) occurs when symbols in a high-speed digital signal overlap, leading to signal distortion that makes it difficult for the receiver to distinguish between individual bits. As high-frequency signals lose energy, edges in the waveform become smeared, resulting in overlap between successive symbols.

Pre-Emphasis and De-Emphasis

Pre-emphasis and de-emphasis are common equalization techniques applied at the transmitter to balance signal frequencies. In *pre-emphasis*, higher-frequency components are boosted,

counteracting the natural high-frequency attenuation of the transmission line. Conversely, *de-emphasis* selectively attenuates low-frequency components, effectively increasing the relative strength of high frequencies.

Chapter 3

Driver Overview

3.1 Voltage-Mode Logic Drivers

Voltage-Mode Logic (VML) drivers are commonly used in high-speed digital systems due to their efficiency, speed, and simplicity. Unlike Current-Mode Logic (CML) drivers, which rely on constant current to drive signals, VML drivers switch between high and low voltage levels to represent the logic states [9].

Key Characteristics

- **Low Power Consumption**: VML drivers typically consume less power than current-mode drivers since they only switch between two voltage levels instead of continuously sourcing or sinking current.
- **High Speed**: VML drivers offer a straightforward and efficient approach to representing digital signals, allowing them to achieve high switching speeds.
- **Compact Design**: The simplicity of VML drivers typically results in fewer components, reduced circuit complexity, lower parasitic effects, and a smaller die area.
- **Signal Integrity Limitations**: Since VML drivers rely on voltage levels rather than a continuous current, they can be more susceptible to noise and signal integrity issues over longer transmission lines or in noisy environments.

Process of Operation

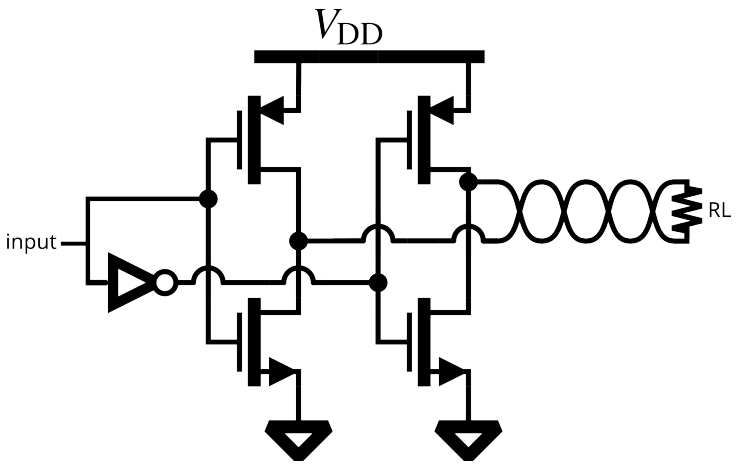

Figure 3.1: Simplified VML Driver Circuit

The circuit in Figure 3.1 illustrates the operation of a VML driver, which uses transistor switching to drive the load resistor R_L. When the input signal is high, the upper right PMOS and bottom left NMOS transistors conduct, allowing current to flow from the source, through the transmission line, across the load resistor, and then to ground in one direction. Conversely, when the input signal is low, the other two transistors activate, reversing the current flow direction across the load.

Differential signaling, shown in Figure 3.2, is achieved by splitting the input into an inverted signal. This approach allows for common-mode rejection, where the two signals, 180 degrees out of phase, cancel out noise and other external interferences common to both signals.

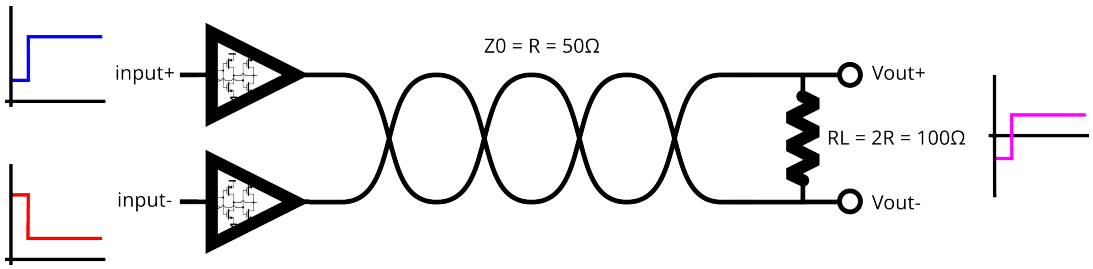

Figure 3.2: Differential signaling

3.2 Existing Architecture

This section provides an overview of the foundational structures used in the transmit driver design. Understanding these baseline structures is crucial for guiding the development of an effective solution in later sections.

Source and Sink Structure Array

The alternating source and sink structures in Figure 3.1 can be extended into an array, which increases the overall drive strength by distributing the load across multiple transistors. Figure 3.3 shows an example of this structure extended into an array of transistors, allowing the circuit to drive larger currents.

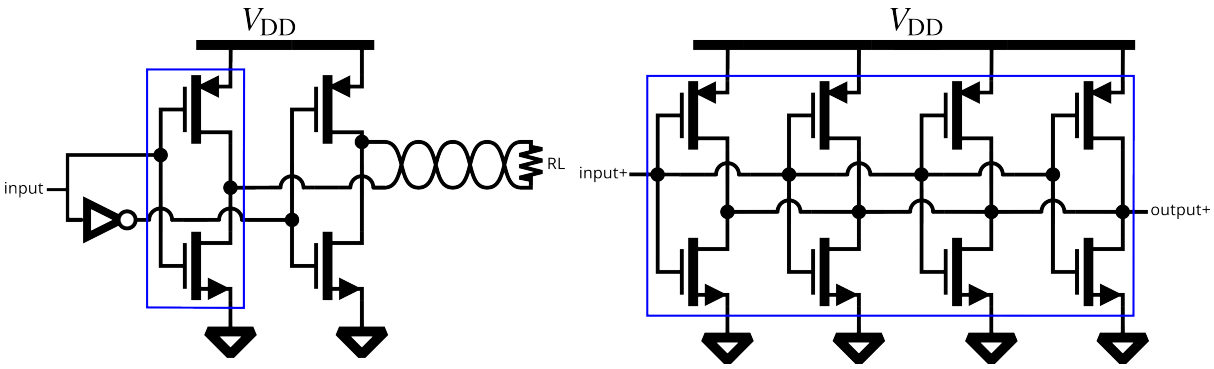

Figure 3.3: Source and Sink Structure Array

Modular Unit Cell Architecture

In this design, each array functions as a unit cell, which can be further extended to a larger array of unit cells. This modular approach, shown in Figure 3.4, simplifies grouping and control of the driver circuit, allowing manageable increases in drive strength. It also supports efficient layout and ensures consistent performance across the circuit.

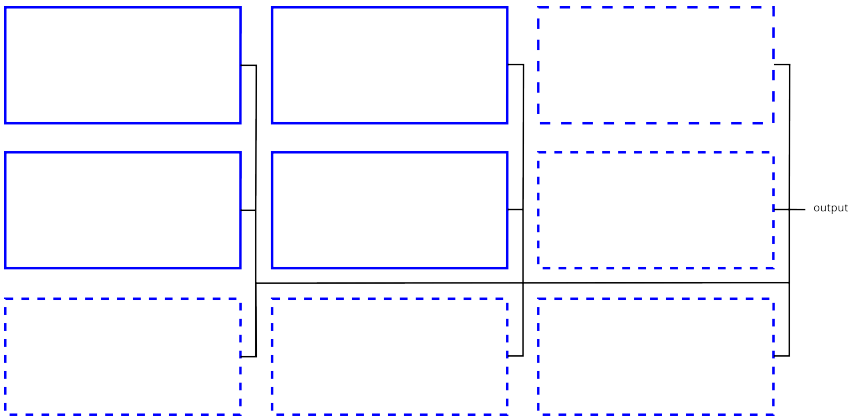

Figure 3.4: Array of Unit Cells

Feeding some of the unit cells with the inverse input enables control over the amplitude by adjusting the output bias, allowing for different voltage swings.

Output Impedance Control

Control over output impedance is achieved by incorporating enable signals within unit cells, as illustrated in Figure 3.5.

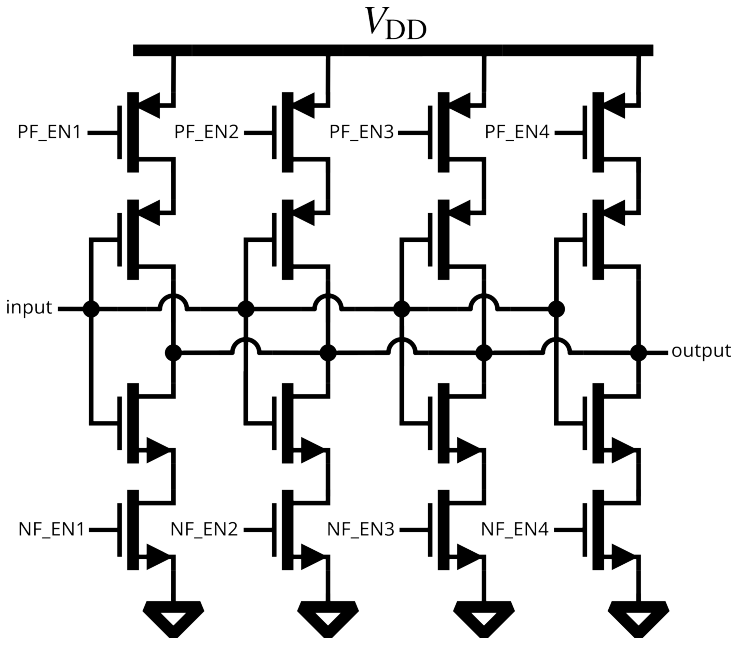

Figure 3.5: Enable Signals within Array of Unit Cells

Increasing the number of transistors switched on reduces the overall output impedance, as the on-resistance of the transistors is effectively in parallel. Figure 3.6 demonstrates this effect using the digital model.

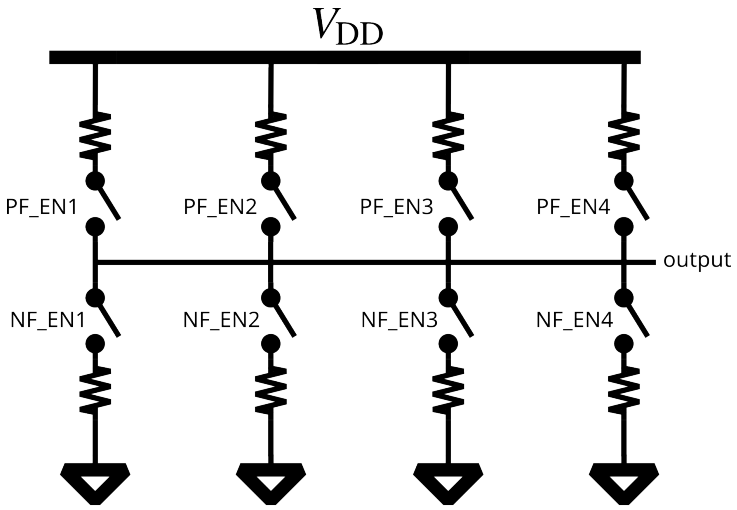

Figure 3.6: Digital Model of Output Impedance Control

It should be noted that the control signals are combined with the input signal, meaning the input must also swing in the direction of the enabled transistor for it to turn on.

Chapter 4

Design Requirements

This chapter focuses on defining the specific technical requirements necessary to ensure the reliability of the design.

4.1 Impedance Mismatch Tolerance

One of the essential limits in ensuring that the driver performs reliably is how much deviation from the ideal impedance can be tolerated before reflections become problematic.

The graph in Figure 4.1 illustrates how the reflection coefficient varies with impedance, assuming a characteristic impedance of $Z_0 = 50\,\Omega$. As shown, the relationship between the impedance deviation from Z_0 and the reflection coefficient is relatively linear.

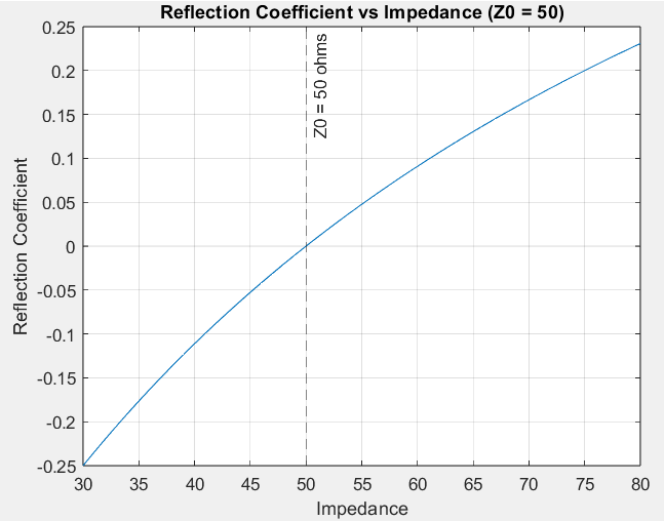

Figure 4.1: Reflection Coefficient as a Function of Impedance for $Z_0 = 50\,\Omega$

To quantify the effects of these reflections, we can assume that all power is either reflected or transmitted:

$$|S_{11}|^2 + |S_{21}|^2 = 1.$$

Thus, given a return loss, we can also calculate the insertion loss that corresponds to it.

The graph below (Figure 4.2) shows that a return loss of around 12 dB and higher results in relatively low losses. We can use return loss bounds up to around 15 dB (where anything more becomes unrealistic to achieve) to calculate various parameters, including the impedance lower and upper bounds, as shown in Table 4.1.

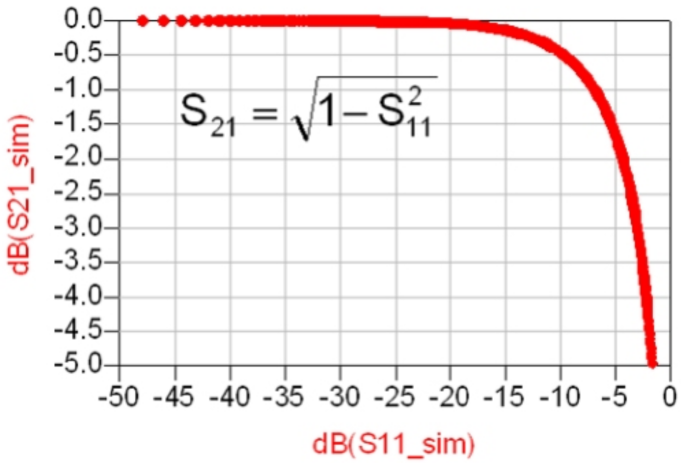

Figure 4.2: Relationship between S_{11} and S_{21} in dB for a low-loss interconnect [10].

Return loss	**12 dB**	**13 dB**	**14 dB**	**15 dB**
Reflection coefficient Γ	0.251	0.224	0.200	0.178
Reflected power $\|\Gamma\|^2$	6.31%	5.01%	3.98%	3.16%
Insertion loss	0.28 dB	0.22 dB	0.18 dB	0.14 dB
Impedance lower bound	29.92 Ω	31.71 Ω	33.37 Ω	34.90 Ω
Impedance upper bound	83.54 Ω	78.84 Ω	74.93 Ω	71.63 Ω

Table 4.1: Parameters calculated based on return loss bounds.

4.2 Transmit Equalization Implementation

Transmit equalization will largely be achieved by pre-emphasis, enabled by the amplitude control inherent in the design. By applying a delay and inversion to the signal and adding it back to the original signal with the appropriate weight, the transition of the signal expanding to adjacent signals (ISI) can be avoided. Figure 4.3 demonstrates this effect.

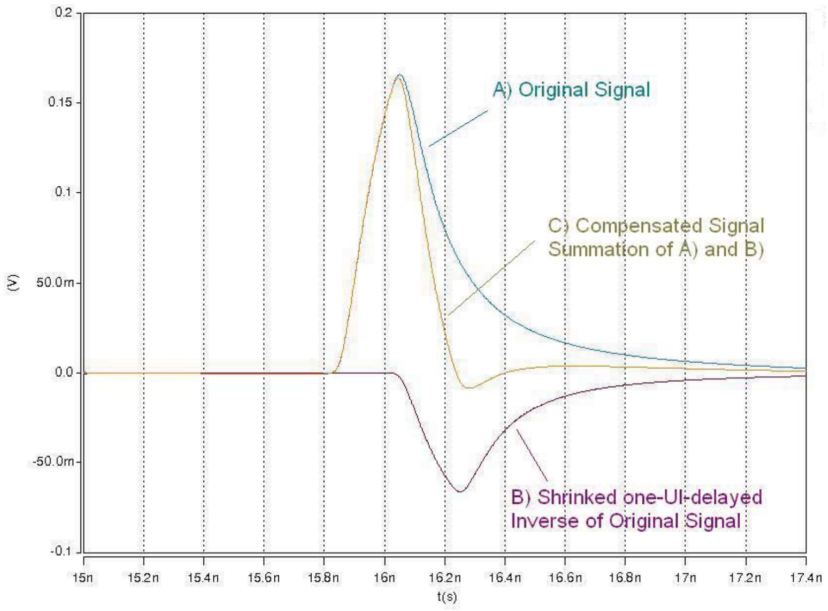

Figure 4.3: ISI Compensation with Pre-Emphasis [8].

To achieve the optimal channel loss compensation, a number of different delays, weights, and polarities can be combined. Thereby, the pre-emphasis implementation essentially operates like a finite impulse response (FIR) filter, where ”taps” correspond to signals at various unit delays. In the frequency domain, pre-emphasis amplifies high-frequency components at each data transition.

Chapter 5

Preliminary Design

5.1 Overview

This chapter discusses a preliminary design for the impedance sensing mechanism. The design centers around monitoring the voltage at the node located at the entrance of the transmission line, V_x, as depicted in Figure 5.1.

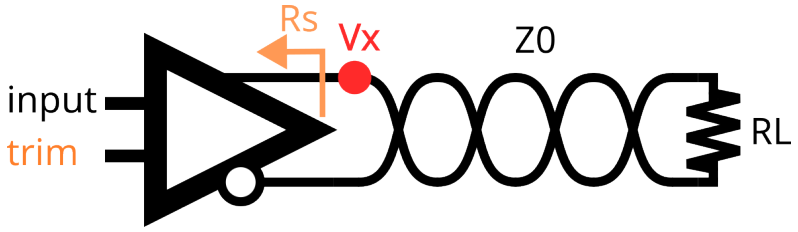

Figure 5.1: Transmit driver with monitored node V_x at the transmission line entrance.

Matched Impedance Condition

When the driver is impedance-matched to both the transmission line and load, the voltage at this node will be $\frac{3}{4}$ of the output voltage swing. This relationship is illustrated in the simplified model of the transmission line with a matched load in Figure 5.2.

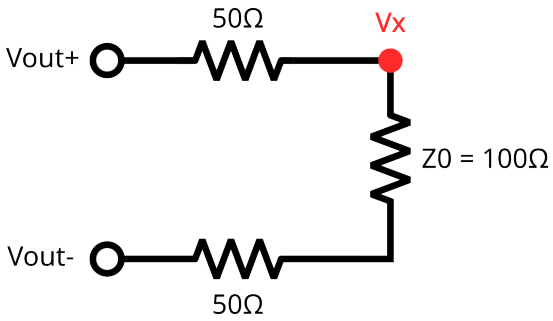

Figure 5.2: Simplified model of the matched system.

In this configuration, the voltage at V_x is calculated as:

$$V_x = \frac{3}{4}(V_{\text{out+}} - V_{\text{out-}})$$

Effect of Impedance Mismatch

When there is a mismatch in the output impedance:

- For $R_s > 50\,\Omega$:
$$V_x < \frac{3}{4}(V_{\text{out+}} - V_{\text{out-}})$$
- For $R_s < 50\,\Omega$:
$$V_x > \frac{3}{4}(V_{\text{out+}} - V_{\text{out-}})$$

This is attributed to an increased or decreased voltage drop across R_s, directly proportional to the impedance mismatch.

Reference Voltage

The monitored node V_x can then be compared to a stable reference voltage, V_{ref}, generated using the same voltage divider proportions as in the matched configuration. As shown in Figure 5.3, this reference voltage divider would operate in the kilo-ohm range to draw a minimal amount of current.

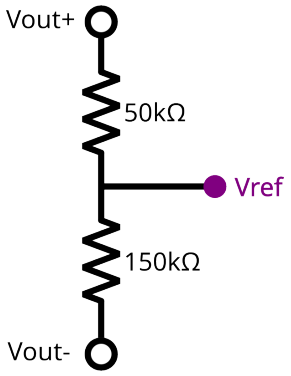

Figure 5.3: Circuit generating the reference voltage V_{ref}.

5.2 Simulations

To evaluate the proposed solution, SPICE simulations were conducted to analyse the behaviour of the system under various configurations.

Setup

The SPICE circuit, shown in Figure 5.4, incorporates a transmission line with inductive and capacitive elements much larger than real-world values for an exaggerated effect. The source voltages V_1 and V_2 generate differential pulse outputs, and source resistors R_s+ and R_s- represent the output impedance of the differential drivers. A matched load of $100\,\Omega$ is applied at the receiving end.

The reference voltages $V_{\text{ref+}}$ and $V_{\text{ref-}}$ are generated using a voltage divider circuit with resistors R_3 and R_4, and a hysteresis band of $\pm 30\,\text{mV}$, as shown in the lower portion of the circuit. The output signals *Out1* and *Out2* are generated using behavioural voltage sources B_1 and B_2 that model ideal comparators, comparing the monitored node to the reference voltage. The combination of these output bits indicate whether the impedance is matched, higher, or lower than Z_0.

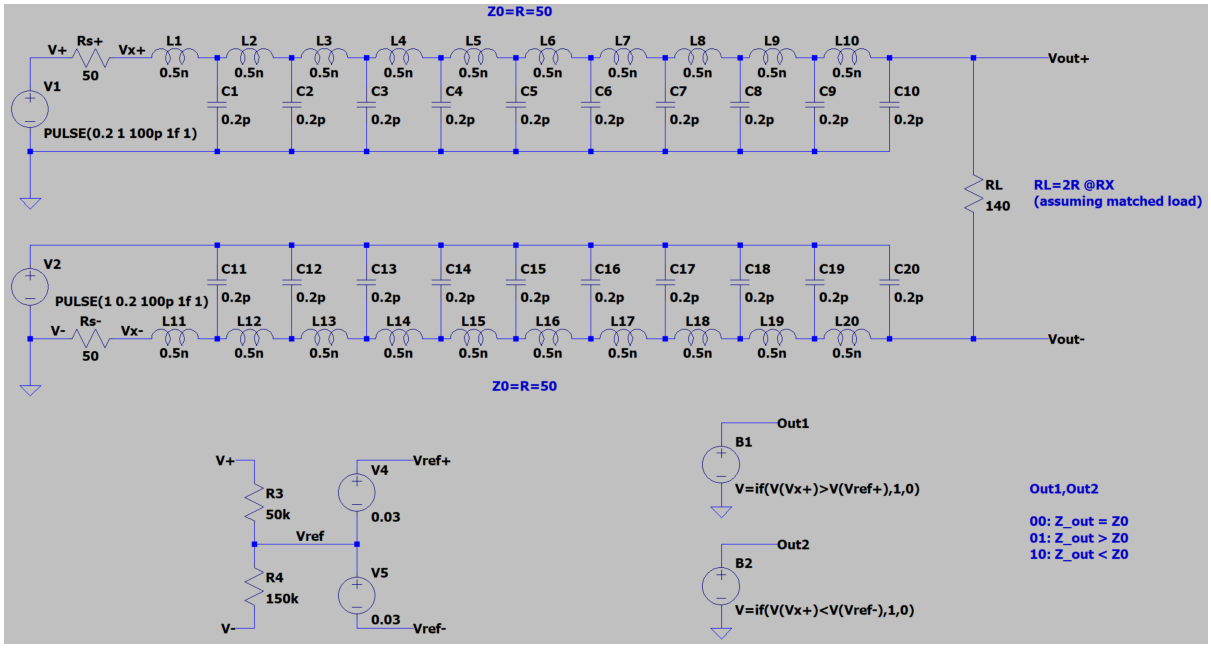

Figure 5.4: SPICE simulation setup.

Simulation Results

The output impedance values tested include $R_s = 50\,\Omega$, $R_s = 70\,\Omega$, and $R_s = 30\,\Omega$, representing matched, high, and low impedance conditions, respectively. The simulation results for different values of the source resistor R_s are shown in Figure 5.5.

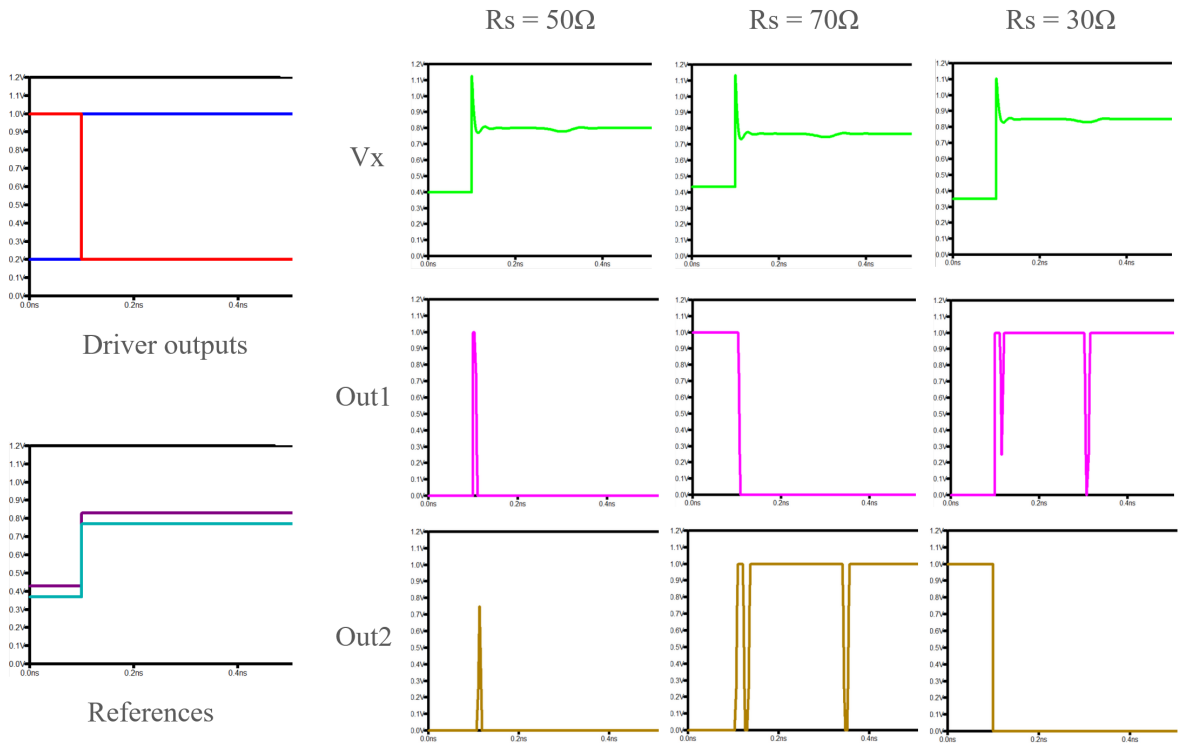

Figure 5.5: SPICE simulation results for different output impedance values.

Observations

While the results of the simulation demonstrate the proposed solution's capability for detecting impedance mismatch, there are a number of observations that need to be considered:

- Large transient at the monitored node V_x directly after the signal transistion. This is because from the perspective of the node, the signal is propagating across the LC segments of the transmission line and does not see the load yet.
- Small changes of V_x which may limit the accuracy of the system, as a larger change will allow detection of even small changes in impedance. Pre-amplifier to the comparator may be needed.
- Ringing of the signal due to reflections that causes the comparator output to switch for a brief moment of time. Smoothing of V_x may be needed.

Chapter 6

Literature Review

6.1 Overview

Traditional approaches to impedance matching involve using fixed termination resistors, which provide a static solution but lack adaptability to varying load conditions. As mentioned previously, variations due to PVT can be substantial on silicon, rendering static solutions impractical. In this context, dynamic impedance sensing and adjustment techniques become essential.

More advanced methods include adaptive impedance tuning, where the system continuously monitors the impedance and adjusts driver settings to maintain optimal matching across different operating environments. These techniques rely on elaborate sensing and calibration strategies to overcome the limitations of static designs.

This review will examine these advanced methods to identify strategies and potential improvements for the preliminary design. Specifically, the next sections explore two key areas: impedance sensing techniques, which evaluate various approaches to detecting the impedance, and related works, which highlight and patented methodologies that align with and inform the preliminary design.

6.2 Impedance Sensing Techniques

Several alternative approaches for the impedance sensor were considered before settling on the preliminary design, which may be revisited in the future. These methods primarily centered around reflectometer designs, which are used to gain information about the reflected signal. This information can then be used to calculate the degree of mismatch and subsequently the

impedance.

- **VSWR-Based Reflectometry:** The Voltage Standing Wave Ratio (VSWR) method measures the ratio of the maximum to minimum voltage amplitudes along a transmission line. This ratio indicates the degree of impedance mismatch, with a VSWR of 1 corresponding to a perfect match. The method involves detecting the locations of voltage peaks and troughs, which arise due to interference between incident and reflected waves. However, at very high frequencies, accurately resolving maxima and minima requires precise sampling. This requirement stems from the shorter wavelengths associated with higher frequencies, leading to closely spaced standing wave patterns. To capture these variations accurately, the sampling system must have a high temporal resolution, increasing the circuit's complexity. Often, directional couplers are used, but they require significant physical space due to the need for tightly coupled transmission lines over a specific length. The size constraint makes achieving the required coupling and isolation impractical for integration in an on-chip environment [11].

- **Time-Domain Reflectometry (TDR):** By analyzing the time delay and amplitude of the reflections, TDR can identify the location and severity of impedance mismatches along the line. While effective for providing spatial resolution, which other methods lack, this level of detail is unnecessary for this application. Moreover, implementing TDR would require an extremely fast sampling circuit, with a sampling rate significantly higher than the signal frequency to accurately resolve the reflections. This requirement makes the TDR circuit large, complex, and unsuitable for on-chip implementation [12].

- **S-Parameter Reflectometry:** This method measures the scattering parameters (S_{11}, S_{21}, etc.) to evaluate impedance mismatches and characterize how signals are reflected and transmitted through a system. S-parameter reflectometry is highly accurate and provides both amplitude and phase information, making it comprehensive for diagnosing and addressing impedance mismatches. However, implementing this method typically requires a Vector Network Analyzer (VNA), a sophisticated instrument that combines precision signal generation and phase-sensitive detection across a wide frequency range. VNAs also often rely on external components, such as calibration kits, directional couplers, and impedance-matching networks. This complexity, along with their size, makes VNAs impractical for on-chip integration [13].

6.3 Related Works

Many approaches utilising a VML driver with programmable unit cells similar to the existing design in this project rely on dummy branches to implement calibration [14] [15] [16] [17]. Dummy branches simulate different impedance states and calibrate the system based on these simulated values. While effective, this approach has a reliance on an external resistor to provide a stable and precise reference impedance to provide accurate calibration of the dummy branches and the overall system. External components provide greater design flexibility as they are not constrained by the limitations of on-chip fabrication processes. Most notably, their ability to be more accurate and stable across temperature ranges. While using external components falls outside the scope of this project, as the existing architecture and requirements mandate a fully on-chip driver, they still offer valuable insights that can inform the preliminary design. For example, the adaptive algorithms themselves are relevant and provide a foundation for implementing the logic. Hence, these papers are noted for future reference as the focus of this initial phase is to ensure a working solution for the impedance sensor first, since there is little value in working on the algorithm if that does not function correctly.

Two relevant patents, EP0463316B1 and US9520842, provide foundational methodologies that can be synthesised and adapted to meet the unique requirements of this design.

EP0463316B1: Self-Adjusting Impedance Matching Driver [18]

This patent describes a dynamic impedance matching technique that employs a comparator-driven iterative adjustment process, similar to the preliminary design. While the design in this patent focuses on a single-ended driver, both designs share the key principle of monitoring the node at the entrance of the transmission line to determine impedance mismatches.

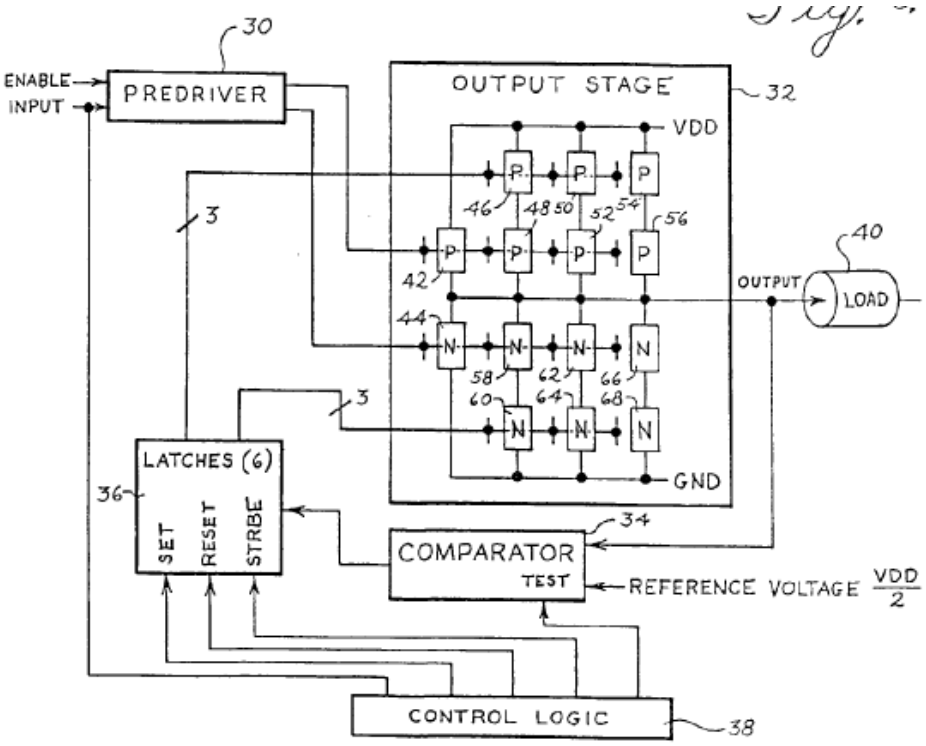

Figure 6.1: Circuit for Dynamic Impedance Matching.

The patent outlines its initial calibration process as follows:

1. All parallel transistors are initially turned on to provide the minimum output impedance.
2. A test signal is applied to the driver, and the output voltage is allowed to stabilize.
3. A comparator evaluates the output voltage against a reference value ($V_{DD}/2$).
4. If the impedance is too low, transistors are progressively turned off using a successive approximation algorithm.
5. This process is repeated for both transitions (rising and falling) to ensure accurate calibration.

The design incorporates a digital latch-based control system to store the states of the driver units. These latches act as a memory element. By selectively enabling or disabling specific driver units, the system achieves fine-grained control over the output impedance.

The successive approximation algorithm ensures reliable performance by iteratively adjusting the impedance until a match is achieved. This algorithm operates by systematically narrowing down the impedance mismatch through a binary search-like process, activating or

deactivating transistors in each step. Such an approach minimises the number of iterations required to converge on the optimal impedance setting, making it both time-efficient and computationally simple.

The need to calibrate for both transitions (rising and falling) ensures symmetry, a principle that is integral to differential drivers. As each transistion involves different signal paths within the driver circuitry, impedance mismatches can occur.

US9520842: Differential Driver for Adaptive Calibration [19]

This patent introduces a method for differential drivers to maintain a balanced output impedance. Symmetry is important in a differential pair to for proper operation, to reduce return loss, and minimise electromagnetic interference (EMI).

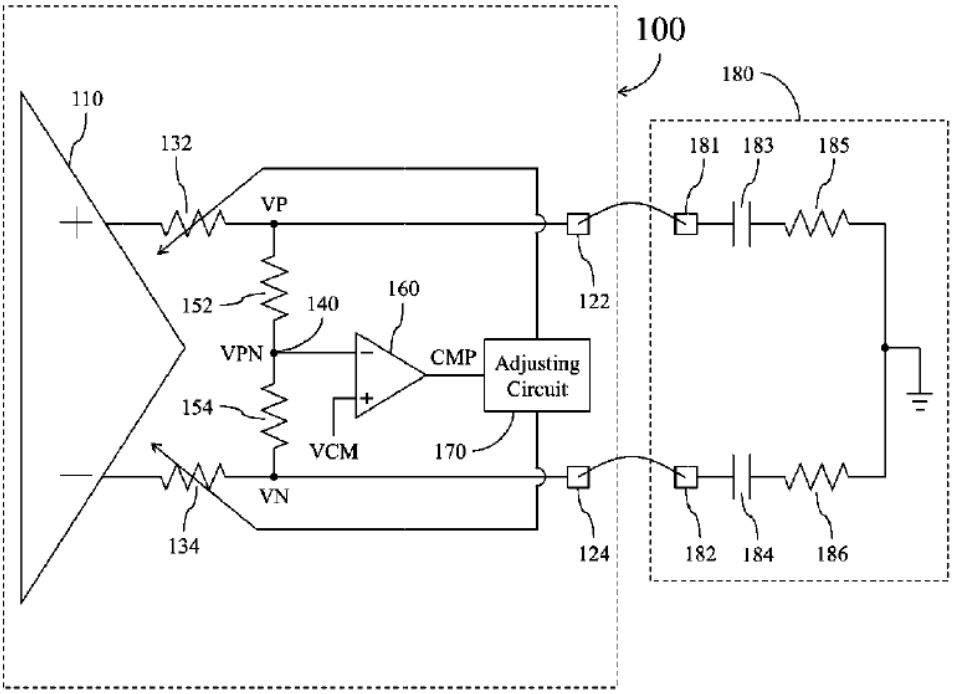

Figure 6.2: Circuit for Ensuring Driver Symmetry.

The process involves:

1. Adjustable resistors on the differential pair paths, which allow fine-tuning of the output impedance.

2. A comparator that compares the divided voltage at an internal node with a reference voltage to detect asymmetry.

3. An adjustment circuit that dynamically modifies the resistances to balance the impedance.

While there is other prior art that use a similar method [20], this is the most simple as beyond implementing the logic, it only requires a single comparator and two resistors.

Gap Analysis and Conclusion

Overall, the majority of prior work focuses on single-ended drivers or external calibration techniques, leaving a gap in solutions for differential drivers with fully integrated on-chip designs. This project addresses that gap by developing an on-chip impedance matching solution specifically tailored for differential drivers operating at GHz frequencies. A key innovation is the adaptation of established methodologies to overcome the constraints of on-chip integration, particularly in mitigating PVT variations without relying on external components. Additionally, existing literature often lacks detailed discussions on adaptive methods that simultaneously address static mismatches and dynamic variations in real time.

Chapter 7

Future Work

In the proposed work plan, key phases and tasks have been identified to incrementally build upon the preliminary design.

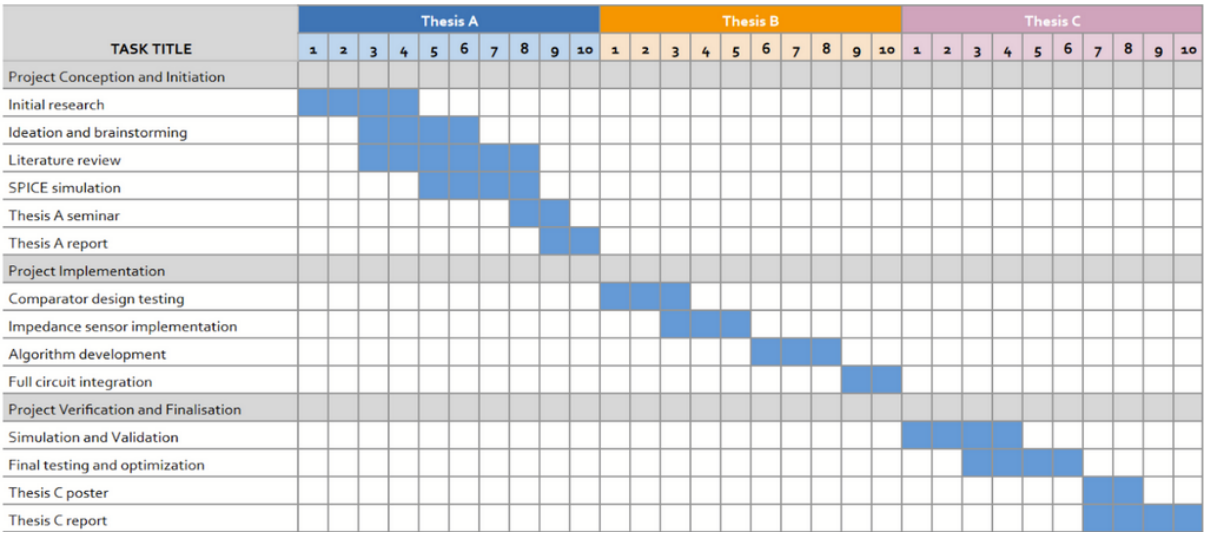

Figure 7.1: Future Work Gantt Chart.

Comparator Testing and Impedance Sensor Implementation

In the immediate future, the focus will be on refining a simple dynamic latching comparator design, then integrating it with the impedance-sensing circuit of the preliminary design. This includes verifying the accuracy of the sensing mechanism under varying load conditions, and ensuring compatibility with the existing driver design's controls.

Algorithm Development

An adaptive algorithm will be developed that takes the comparator's output to inform the existing driver design's controls. The algorithm will undergo iterative testing and optimization to align with transmit equalisation and dynamic performance requirements.

System Integration

Following the successful development of the individual modules, the next stage involves full system integration. The emphasis will be on seamless communication between the comparator, impedance-sensing circuitry, and the control logic. Extensive testing will be conducted to identify and mitigate any inter-module incompatibilities, ensuring reliable performance at the system level.

Simulation and Verification

The integrated system will be subjected to comprehensive simulations to validate its performance under various PVT conditions. This phase aims to assess the dynamic impedance-matching capabilities and ensure the system's stability and efficiency over a broad operating range.

Final Implementation and Optimisation

The final stages of the project involve fabrication-level considerations, such as layout design and parasitic extraction, to evaluate the circuit in its physical form. Optimisation efforts will focus on enhancing performance, reducing power consumption, minimising area.

Validation and Documentation

The project will conclude with a detailed validation process including a review with experienced professionals or senior engineers. The final deliverables will include a comprehensive report, a detailed technical poster for dissemination, and all necessary documentation for future improvements or research based on this work.

Bibliography

[1] Altium. Understanding signal reflections for high-speed design. https://resources.altium.com/p/understanding-signal-reflections-for-high-speed-design, 2024. Altium Resources.

[2] Wikipedia contributors. Signal integrity. https://en.wikipedia.org/wiki/Signal_integrity, 2024. Wikipedia.

[3] Hoon Jung, Changhwan Park, and Byungho Park. PVT variation detection and compensation methods for high-speed systems. *ResearchGate*, 2014.

[4] Analog Devices. Impedance matching. https://www.analog.com/en/resources/glossary/impedance-matching.html.

[5] PSpice. Transmission line modeling. https://www.pspice.com/resources/application-notes/transmission-line-modeling.

[6] University of Vermont. S-parameters: Measuring high-frequency networks. https://www.uvm.edu/~muse/modules/RFH/MUSE_S-parameters_081003.pdf.

[7] James Perry. The impact of microarchitecture on signal integrity. https://www.cs.unc.edu/~jp/Micro97.pdf.

[8] Altera. Understanding the pre-emphasis and linear equalization features in stratix iv gx devices. https://cdrdv2-public.intel.com/654771/an602.pdf, 2012.

[9] Silvino Spalermo. Transmit circuits. https://people.engr.tamu.edu/spalermo/ecen689/lecture11_ee689_tx_circuits.pdf. Lecture slides, Texas A&M University.

[10] John Horn. Why connector return loss causes signal problems. https://www.connectortips.com/why-connector-return-loss-causes-signal-problems/, 2022. Connector Tips.

[11] High-power microstrip directional couplers: Design and challenges for on-chip integration, 2023.

[12] J. Krampmeier. Building a poor man's time domain reflectometer. https://www.eevblog.com/forum/projects/building-a-poor-man_s-time-domain-reflectometer/, April 2016.

[13] ProtoExpress. S-parameters measurement using a vector network analyzer (vna). https://www.protoexpress.com/blog/s-parameters-measurement-vector-network-analyzer/, 2024.

[14] Ming Zheng, Wen-bin Liu, Xia Wu, Guo-jin Wang, and Lu Zhang. A 6.4-gbps voltage-mode transmitter with a dynamic impedance calibration technique. *Journal of Semiconductors*, 33(4):045003, 2012.

[15] Kwang-Hyun Kwak, Jung-Hoon Ra, Hyung-Jun Moon, Seong-Ho Hong, and Oh-Kyong Kwon. A low-power two-tap voltage-mode transmitter with precisely matched output impedance using an embedded calibration circuit. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 63(6):573–577, 2016.

[16] L. Tai, M. T. Mustaffa, and K. H. Chan. A two-tap voltage-mode transmitter with adaptive de-emphasis and impedance self-calibration in 45 nm cmos. In *2012 4th International Conference on Intelligent and Advanced Systems (ICIAS2012)*, pages 174–179. IEEE, 2012.

[17] Xu Bai, Jianzhong Zhao, and Yumei Zhou. A high precision output impedance calibration technique for sst transmitter. *Journal of Circuits, Systems and Computers*, 29(5):2050025, 2019.

[18] Alice Irene Biber and Douglas Willard Stout. Self-adjusting impedance matching driver, 1996. European Patent Office. Filed April 25, 1991. Granted July 3, 1996.

[19] Chao-Cheng Lee, Jian-Ru Lin, Chien-Ming Wu, and Shih-Wei Wang. Transmission line driver circuit for adaptively calibrating impedance matching, 2016. Filed: September 1, 2015. Granted: December 13, 2016.

[20] Chao-Cheng Lee, Jian-Ru Lin, Shih-Wei Wang, and Guan-Hong Ke. Transmission line driver circuit for automatically calibrating impedance matching, 2016. Filed: September 1, 2015. Published: March 31, 2016. Priority date: September 30, 2014 (TW).

Appendix 1: MATLAB Code

This appendix contains MATLAB code used for generating the reflection coefficient graph and calculating impedance parameters.

Code for Reflection Coefficient Graph

The following MATLAB code generates a plot of the reflection coefficient as a function of impedance, assuming a characteristic impedance of $Z_0 = 50\,\Omega$.

```
Z0 = 50;
R = 30:80;
gamma = (R - Z0) ./ (R + Z0);

plot(R, gamma);
hold on;

xline(Z0, '--', 'Z0 = 50 ohms');

xlabel('Impedance');
ylabel('Reflection Coefficient');
title('Reflection Coefficient vs Impedance (Z0 = 50)');

grid on;
hold off;
```

Code for Calculating Impedance Parameters

The following MATLAB function calculates design parameters, including insertion loss, reflection coefficient, reflected power, and impedance bounds, based on a given return loss in dB.

```
function calculate_impedance_params(return_loss_dB)
    % This function takes return loss in dB and calculates the insertion loss,
    % reflection coefficient, reflected power, and impedance bounds.

    Z0 = 50;  % Characteristic impedance (ohms)

    % Calculate reflection coefficient (Gamma)
    Gamma = 10^(-return_loss_dB / 20);

    % Calculate reflected power |Gamma|^2 as a percentage
    reflected_power = (Gamma^2) * 100;

    % Calculate insertion loss (S21)
    S21 = sqrt(1 - Gamma^2);
    insertion_loss_dB = -20 * log10(S21);

    % Calculate impedance bounds
    impedance_upper = Z0 * (1 + Gamma) / (1 - Gamma);
    impedance_lower = Z0 * (1 - Gamma) / (1 + Gamma);

    % Display the results
    fprintf('Return Loss: %.2f dB\n', return_loss_dB);
    fprintf('Reflection Coefficient (Gamma): %.3f\n', Gamma);
    fprintf('Reflected Power: %.2f%%\n', reflected_power);
    fprintf('Insertion Loss: %.2f dB\n', insertion_loss_dB);
    fprintf('Impedance Upper Bound: %.2f ohms\n', impedance_upper);
    fprintf('Impedance Lower Bound: %.2f ohms\n', impedance_lower);
end
```

Appendix 2: Risk Management Form

HS017

HS Risk management form

For additional information refer to HS329 Risk Management Procedure

Faculty/Division:			School/Unit: Electrical Engineering & Telecommunications	
Document number	Initial Issue date	Current version	Current Version Issue date	Next review date

Risk management name Ergonomic issues from sitting in chair

Form completed by	Jamie Mo	*Signature*	*Date* 18/11/2024
Responsible supervisor/ authorising officer		*Signature*	*Date*

Identify the activity and the location of the activity

Description of activity Working on design tasks.

Description of location At home, university and the office.

Identify who may be at risk from the activity:

This may include fellow workers, visitors, contractors and the public. The types of people may affect the risk controls needed and the location may affect the number of people at risk

Persons at risk

How they were consulted on the risk

List legislation, standards, codes of practice, manufacturer's guidance etc used to determine control measures necessary

Work Health and Safety Act 2011
Work Health and Safety Regulation 2011

Identify hazards and control the risks.
1. An activity may be divided into tasks. For each task identify the hazards and associated risks. Also list the possible scenarios which could sooner or later cause harm.
2. Determine controls necessary based on legislation, codes of practice, Australian standards, manufacturer's instructions etc.
3. List existing risk controls and any additional controls that need to be implemented
4. Rate the risk once all controls are in place using the matrix in HS329 Risk Management Procedure

SHADED GREY AREAS
If you need to determine whether it's reasonably practicable to implement a control, based on the risk complete the shaded grey columns

Feel free to resize the boxes to suit your situation/the amount of text you need to use

Task/ Scenario	*Hazard*	*Associated harm*	*Existing controls*	*Any additional controls required?*	*Risk Rating*			*Cost of controls (in terms of time, effort, money)*	*Is this reasonably practicable* Y/N
					C	*L*	*R*		
Sitting	Poor work-station set-up		• -Take frequent breaks -Enhance ergonomic setup	No				N/A	N/A
			•						
			•						
			•						

RISK RATING METHODOLOGY AND MATRIX

Consider the Consequences	Consider the Likelihood
Consider: What type of harm could occur (minor, serious, death)? Is there anything that will influence the severity (e.g. proximity to hazard, person involved in task etc.). How many people are exposed to the hazard? Could one failure lead to other failures? Could a small event escalate?	Consider: How often is the task done? Has an accident happened before (here or at another workplace)? How long are people exposed? How effective are the control measures? Does the environment effect it (e.g. lighting/temperature/pace)? What are people's behaviours (e.g. stress, panic, deadlines) What people are exposed (e.g. disabled, young workers etc.)?
5. Severe: death or permanent disability to one or more persons	**A. Almost certain:** expected to occur in most circumstances
4. Major: hospital admission required	**B. Likely:** will probably occur in most circumstances
3. Moderate: medical treatment required	**C. Possible:** might occur occasionally
2. Minor: first aid required	**D. Unlikely:** could happen at some time
1. Insignificant: injuries not requiring first aid	**E. Rare:** may happen only in exceptional circumstances

Calculate the Risk

1.Take the consequences rating and select the correct column

2.Take the likelihood rating and select the correct row

3. Select the risk rating where the two ratings cross on the matrix below.

VH = Very high, H = High, M = Medium, L = Low

		CONSEQUENCES				
		1	2	3	4	5
LIKELIHOOD	A	M	H	H	VH	VH
	B	M	M	H	H	VH
	C	L	M	H	H	VH
	D	L	L	M	M	H
	E	L	L	M	M	M

Risk level	Required action
Very high	**Act immediately**: The proposed task or process activity must not proceed. Steps must be taken to lower the risk level to as low as reasonably practicable using the hierarchy of risk controls
High	**Act today:** The proposed activity can only proceed, provided that: (i) the risk level has been reduced to as low as reasonably practicable using the hierarchy of risk controls and (ii) the risk controls must include those identified in legislation, Australian Standards, Codes of Practice etc. and (iii) the document has been reviewed and approved by the Supervisor and (iv) a Safe Working Procedure or Safe Work Method has been prepared and (v) the supervisor must review and document the effectiveness of the implemented risk controls
Medium	**Act this week**: The proposed task or process can proceed, provided that: (i) the risk level has been reduced to as low as reasonably practicable using the hierarchy of controls and (ii) the document has been reviewed and approved by the Supervisor and (iii) a Safe Working Procedure or Safe Work Method has been prepared.
Low	**Act this month:** Managed by local documented routine procedures which must include application of the hierarchy of controls.

List emergency procedures and controls **List emergency controls for how to deal with fires, spills or exposure to hazardous substances and/or emergency shutdown procedures**

Implementation			
Additional control measures needed:	**Resources required**	**Responsible person**	**Date of implementation**

REVIEW			
Scheduled review date:			
Are all control measures in place?			
Are controls eliminating or minimising the risk?			
Are there any new problems with the risk?			
Review by: (name)			
Review date:			

Acknowledgement of Understanding

All persons performing these tasks must sign that they have read and understood the risk management (as described in HS329 Risk Management Procedure).

Note: for activities which are low risk or include a large group of people (e.g. open days, BBQ's, student classes etc), only the persons undertaking the key activities need to sign below. For all others involved in such activities, the information can be covered by other methods including for example a safety briefing, induction, and/or safety information sheet (ensure the method of communicating this information is specified here)

Risk management name and version number:	**I have read and understand this risk management form**	
Name	Signature	Date